

ENERGY EFFICIENT CARRY SKIP ADDER USING SKIP LOGIC IN VARIOUS VOLTAGE LEVELS

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ABSTRACT

A carry skip adder (CSKA) structure has the high speed and very low power consumption. The speed of the structure is achieved by concatenation of all the blocks. The incrementation blocks are used to improve the efficiency of the carry skip adder structure. In existing method multiplexer logic is used, the proposed structure uses the AND-OR-Invert (AOI) and OR-AND-Invert (OAI) for the skip logic. The carry skip adder structure is realized with both fixed stage size and variable stage size where the delay is reduced, and speed is improved. A hybrid variable latency extension lowers the power consumption without affecting the speed of the circuit. The results are obtained using XILINX and it gives 42% and 37% improvements in the delay and energy of the structures. In addition to this structure, the power–delay product was low among all the structures, while having its energy–delay product was almost same as that of the conventional structure. Simulations on the proposed structure by using hybrid variable latency CSKA reduces the power consumption compared with the previous works and it produces a high speed.

KEYWORDS: Carry Skip Adder (CSKA), AOI, OAI, Energy Efficient, High Performance, Hybrid Variable Latency Adders

I. INTRODUCTION

Low power adder circuits have become very important in VLSI industry. Adder circuit is one of the main building block in DSP processor. Adder is the main component in most of the arithmetic unit. Addition is a fundamental operation for any digital system, DSP or control system. The fast operation of a digital system is having great influenced by the performance of the resident adders. Adders plays important component in digital systems because of the more number for use in other basic digital operations such as subtraction, multiplication and division. Hence, the improving performance of the digital adder increases the execution of various binary operations in a circuit consisting of different blocks. The appearance of the digital circuit block is gauged by analyzing its power dissipation, layout area and its operating speed. There are many works on the subject of optimizing the speed and power of these units, which has been reported in [2]–[9]. Obviously, it is extremely possible to achieve higher speeds at low-power and energy consumptions, which is one of the challenge for the designers of general purpose processors.

In existing method, we are using multiplexer logic in which the number of gate count is more. The power consumed by the carry skip adder using multiplexer logic is more and critical path delay is high. The ripple carry adder is constructed by cascading number of full adders (FA) blocks in series. One complete full adder is responsible for the addition of two binary digits at different stage of the ripple carry. The carry output of one stage is fed directly to the

carry-in of the next stage. A number of full adders outputs is added to the ripple carry adder circuit or ripple carry adders of different sizes may be cascaded in order to accommodate the binary vector strings of larger sizes of adders. For an n-bit parallel adder, it requires n computational elements (FA). The carry is propagated in a serial computation [1]. Hence, delay is more as the number of bits is increased in RCA.

The rest of this paper is organized as follows. Section II discusses related work on the proposed CSKA structure for improving the speed and for increasing the efficiency of adders. In Section III, ripple carry structure is explained, while Section IV describes the skip logic of CSKA structure. The incrementation block structure is suggested in Section V. The results and discussion of one stage of proposed structures is discussed in Section VI. Finally, the conclusion is given in section VII.

II. PROPOSED WORK

The focus of this paper is on speed of the carry skip adder structure and the reduction in the critical path Daley. The proposed system contains the ripple carry adder structure with the AOI and OAI compound gates for skip logic. The skip logic reduces the number of gate count in the structure [2]. The speed of the structure is achieved by using skip logic and the delay is reduced. The conventional structure of the CSKA consists of stages containing chain of full adders (FAs) (RCA block) and 2:1 multiplexer (carry skip logic). The RCA blocks are connected to each other through 2:1 multiplexers, which can be used in one or more level structures [11].

The CSKA configuration (i.e., the number of the FAs per stage) has a great impact on the speed of this type of adder [13]. Many methods have been suggested for finding the optimum number of the FAs [1]–[2].

Figure 2.1 shows the adder contains two N bits inputs, A and B, and Q stages. Each stage consists of an RCA block with the size of M_j ($j = 1, \dots, Q$). In this structure, the carry input of all the RCA blocks, except for the first block which is C_i , is zero (concatenation of the RCA blocks). Therefore, hence all the blocks of the structure and execute their jobs simultaneously.

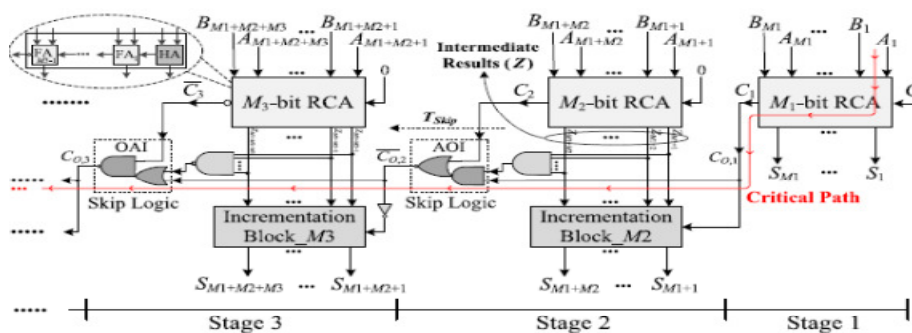


Figure 2.1: Proposed Structure of CSKA

In this structure, when the first block computes the summation of its corresponding input bits (i.e., S_{M1}, \dots, S_1) and C_1 , the other blocks simultaneously compute the intermediate results and also C_j signals. In the proposed structure, the first stage has only one block, which is RCA [3]. The stages 2 to Q consist of two blocks of RCA and incrementation. The incrementation block uses the intermediate results generated by the RCA block and the carry output of the previous stage to calculate the final summation of the stage [5]– [7].

All the RCA blocks, except for the 1st block having zero as carry input. Output carries of the RCA blocks are calculated in parallel.

III. RIPPLE CARRY ADDER

The ripple carry adder structure is constructed by cascading full adders (FA) blocks in series. One full adder is responsible for the adding of the two binary digits at different stage of the ripple carry [9]. The carry out of one stage is fed directly to the carry-input to the next stage. A number of full adders circuits may be added to the ripple carry adder or ripple carry adders of the different sizes may be cascaded in the order which accommodate binary vector strings of larger sizes [7]. For an n-bit parallel adder, it requires n number of computational elements (FA).

The worst-case delay of the RCA is when a carry signal propagates ripples through all the stages of adder chain from the LSB to the MSB, which is approximated by:

$$T = (n-1) t_c + t_s$$

where the t_c is the delay through the carry stage of a different full adder, and t_s is the delay used to compute the sum of the last stage.

IV. SKIP LOGIC

The skip logic contains the AOI (AND OR Invert) and OAI (OR AND Invert) compound gates for skip logic. The gates, which consist of fewer transistors, have lower delay, area, and smaller power consumption compared with those of the 2:1 multiplexer [7]. Note that, in this structure, as the carry propagates through the skip logics, it becomes complemented.

The structure has a considerable lower propagation delay with a slightly smaller area compared with those of the existing one. Note that while the power consumed by the AOI (or OAI) gate are smaller than that of the multiplexer, hence the power consumption of the proposed CI-CSKA is a little more than that of the conventional carry skip adder structure [8]-[9]-[10].

V. INCREMENTATION SCHEMES

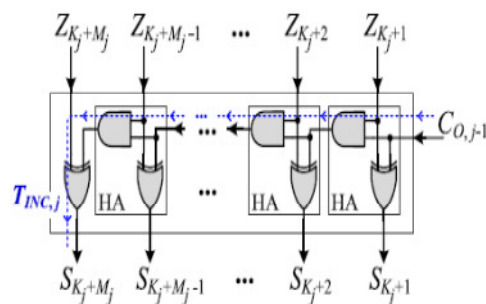


Figure 5.1: Internal Structure of Incrementation Block

The internal structure of the incrementation block, which contains a chain of half-adders (HAs), is shown in Figure 5.1. In addition, note that, to reduce the delay considerably, for computing the carry output of the stage, the carry output of the incrementation block is not used. The incrementation contains AND gate and EX-OR gate. The carry input is fed into the structure and it performs the operation like the half adder.

VI. RESULTS AND DISCUSSIONS

The design proposed in this paper has been developed using MODEL SIMULATOR. ADDERS are a key building block in arithmetic and logic units (ALUs). Low power arithmetic circuits have become very important in VLSI industry. Adder circuit is the main building block in DSP processor. Adder is the main component of arithmetic unit. A complex DSP system involves several adders. Many design styles of adders exist.

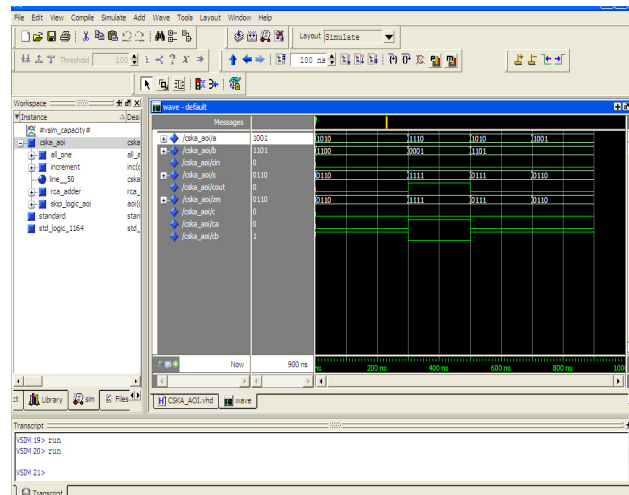


Figure 7.1: Output of an Stage-2 Block in CSKA Structure

The output for single stage is shown in figure 7.1 in which it contains four bit input A and B. The value of Z is obtained by performing the full adder operation for the given set of inputs. The value S is the output value of the incrementation block. The concatenation of all stages increase the speed and improves the efficiency of the circuit.

VII. CONCLUSIONS

In this paper, Carry Skip Adder (CSKA) structure was proposed, which exhibits a higher speed and lower energy consumption compared with the conventional structure. The speed is through the concatenation and efficiency by the incrementation techniques. In addition, AOI and OAI compound gates were exploited for the carry skip logics. The efficiency of the proposed structure for both FSS and VSS was studied. The results also suggested that the CSKA structure is a very good adder for the applications where both the speed and energy consumption are critical. In addition, a hybrid variable latency extension of the structure was proposed which reduces the power without affecting the speed of the structures.

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